

U.S. Department of Commerce, Patent and Trademark Office				Atty. Docket No.		Application No.	
				NS-5127-1D US		10/699,221	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant(s)		Confirmation No.	
Substitute Form PTO 1449				Bulucea, Constantin		2799	
MAY 09 2005				Filing Date		Group	
				31 October 2003		2814	

U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
DF	AA	2002/0074589	06/2002	Benaissa et al.	257	312	
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AA						
	AB						
	AC						
	AD						
	AE						
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	AH						

Foreign Patent Documents							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AI							
	AJ							
	AK							
	AL							
	AM							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
DF	AN	Takeuchi et al, "A New Multiple Transistor Design Methodology for High Speed Low Power SOC's," <u>IEDM Technical Digest</u> , December 2001, pages 22.6.1 - 22.6.7
	AO	
	AP	

Examiner <i>Dasher</i>	Date Considered <i>12/19/05</i>
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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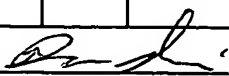
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
DF	AA	4,003,009	01/1977	Watanabe	334	015	
	AB	4,529,994	07/1985	Sakai	357	014	
	AC	5,504,376	04/1996	Sugahara et al.	257	768	
	AD	5,659,185	10/1997	Iwamuro	257	138	
	AE	5,977,591	11/1999	Fratin et al.	257	344	
	AF	6,165,902	12/2000	Praminick et al.	438	653	
	AG	2002/0036311 A1	03/2002	Hattori	257	302	
DF	AH	2003/0178689 A1	09/2003	Maszara et al.	257	407	
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						

Foreign Patent Documents							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
PC	AI	4-199682	07/1992	Japan	257	365		X
	AJ							
	AK							
	AL							
	AM							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)	
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AP	

Examiner <i>De Han</i>	Date Considered <i>12/17/05</i>
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U.S. Department of Commerce, Patent and Trademark Office				Atty Docket No.		Application No.	
				NS-5127-1D US		Unknown	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Applicant		Confirmation No.	
(Use several sheets if necessary)				Constantin Bulucea		Unknown	
				Filing Date		Group	
				Herewith		Unknown	
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
DF	AA	09/903,059		Bulucea			10 July 2001
DF	AB	5,399,893	03/95	Weitzel et al.	257	355	
DF	AC	5,497,028	03/96	Ikeda et al.	257	531	
DF	AD	6,100,770	08/00	Litwin et al.	331	117 FE	
DF	AE	6,166,404	12/00	Imoto et al.	257	279	
	AF						
Foreign Patent Documents							
							Translation
		Document	Date	Country	Class	Subclass	Yes No
DF	AG	6-61446	03/1994	Japan			X
DF	AH	7-226643	10/1995	Japan			X
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
DF	AH	Andreani, et al., "A 1.8-GHZ CMOS VCO Tuned by an Accumulation-Mode MOS Varactor," IEEE Intl. Symposium on Circuits and Systems, 28 - 31 May 2000, pp. I-315 - I - 318.					
DF	AI	Grove, <u>Physics and Technology of Semiconductor Devices</u> (John Wiley & Sons), 1967, pp. 263 - 305.					
DF	AJ	Grove, et al., "Effect of Surface Fields on the Breakdown Voltage of Planar Silicon <i>p-n</i> Junction," <u>IEEE Trans. Electron Devices</u> , vol. ED-14, 1967, pp. 157 - 162.					
DF	AK	Grove, et al., "Surface Effects on <i>p-n</i> Junctions: Characteristics of Surface Space-Charge Regions Under Non-Equilibrium Conditions," <u>Solid-State Electronics</u> , Vol. 9, 1966, pp. 783 - 806.					
DF	AL	Kral, et al., "RF-CMOS Oscillators with Switched Tuning," <u>Procs. IEEE Custom Integrated Circuits Conference</u> , 1998, pp. 555 - 558.					
DF	AM	Lee, <u>The Design of CMOS Radio-Frequency Integrated Circuits</u> (Cambridge Univ. Press), 1998, pp. 37 - 41 and 504 - 514.					
DF	AN	McMahon, et al., "Voltage-Sensitive Semiconductor Capacitors," <u>1958 IRE Wescon Conf. Rec.</u> , Part 3, 19 - 22 August 1958, pp. 72 - 82.					
DF	AO	Moll, "Variable Capacitance With Large Capacity Change," <u>IRE Wescon Conf. Rec.</u> , Vol. 3, 1959, pp. 32 - 36.					
Examiner 		Date Considered 12/19/05					
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					NS-5127-1D US		10/054,653	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant		Confirmation No.	
(Use several sheets if necessary)					Constantin Bulucea		9448	
					Filing Date		Group	
					January 18, 2002		2814	
U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA							
	AB							
	AC							
	AD							
	AE							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AF							
	AG							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
DF	AH	Ng, <u>Complete Guide to Semiconductor Devices</u> (McGraw Hill), 1995, pp. 11 - 22.						
PF	AI	Razavi, <u>Design of Analog CMOS Integrated Circuits</u> (McGraw Hill), 2001, pp. 495 - 525.						
DF	AJ	Rusu et al., "Deep-Depletion Breakdown Voltage of Silicon-Dioxide/Silicon MOS Capacitors," <u>IEEE Trans. Elec. Devs.</u> , March 1979, pp. 201 - 205.						
DF	AK	Rusu et al., "Reversible Breakdown Voltage Collapse in Silicon Gate-Controlled Diodes," <u>Solid-State Electronics</u> , Vol. 23, 1980, pp. 473 - 480.						
PF	AL	Sedra, et al., <u>Microelectronic Circuits</u> , (4th ed., Oxford Univ. Press), 1998, p. 382.						
DF	AM	Svelto, et al., "A Three Terminal Varactor for RF IC's in Standard CMOS Technology," <u>IEEE Transactions on Electron Devices</u> , Vol. 47, 2000, pp. 893 - 895.						
DF	AN	Warner, Jr., et al., <u>Transistors - Fundamentals for the Integrated-Circuit Engineer</u> (John Wiley & Sons), 1983, pp. 320 - 321.						
DF	AO	Wong et al., "A Wide Tuning Range Gated Varactor," <u>IEEE J. Solid State Circs</u> , May 2000, pp. 773 - 779.						
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